IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	10/538,624	Confirmation No.
Applicant	:	Saleh Osman *et al.*	
Filed	:	June 10, 2005	
TC/A.U.	:	2818	
Examiner	:	Earl N. Taylor	
Docket No.	:	**US020555**	
Customer No.	:	65913	
Title	:	Preserving Linearity of an Isolator-Free Power Amplifier by Dynamically Switching Active Devices	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PETITION UNDER 37 CFR 1.47(a)

Sir:

In response to the March 30, 2006 Decision in response to Applicants' petition under 37 CFR 1.47(a) filed on February 9, 2006, Applicants request reconsideration in light of renewed efforts to locate the non-signing inventor, Saleh Osman. These efforts begun in October 19, 2006 were not successful. Attached is a declaration presenting the facts of the renewed effort and a Petition to Revive the above-captioned application.

Applicants believe that a sufficient effort has been made in attempting to obtain signature of the non-signing inventor. Therefore, acceptance of present application with a non-signing inventor under 35 CFR 1.47(a) is earnestly requested.

Please charge any fees other than the issue fee and credit any overpayments to Deposit Account 50-4019

Declaration of Facts Regarding Inventor's Unavailability begins on page 2.

DECLARATION OF FACTS REGARDING INVENTOR'S UNAVAILABILITY

I Peter Stephen Zawilski declare that:

I am managing the prosecution of the above-referenced patent application.

In response to the Decision on Petition of March 30, 2006 rejecting the declaration of the attorney who had prepared the application, Dicran Halajian, I made additional efforts to locate Saleh Osman so that he may sign the Oath and Declaration.

The present application is being prosecuted by NXP, B.V. Previously, Philips Intellectual Property & Standards was managing this case as a part of Koninklijke Philips Electronics, N.V. (KPENV). The NXP organization was spun-off from KPENV on October 1, 2006 as an independent entity.

Mr. Saleh Osman is no longer employed by Koninklijke Philips Electronics, N.V. (KPENV) or NXP, B.V.

1). As described in Exhibit 1, an E-mail dated October 17, 2006, to co-inventors Jarek Lucek and Richard Keenan was sent requesting contact information. Another colleague, Korne Vennema was contacted as well. None these individuals could supply me with information. Mr. Lucek wrote that "Shortly after filing the patents we have let him go." Mr. Osman no longer works for Philips.

2). As shown in Exhibit 2 using the last know address for Mr. Osman, I requested my Assistant, Vilimaina Naga to mail a copy of his application (as was filed on June 10, 2005) with a replacement Oath & Declaration, Cover Letter, a Prepaid Return Envelope (having tracking number EL 995158902 US) and my Business Card via Express Mail from the US Post Office on October 20, 2006 (having a tracking number of EL 995158964 US)

3). As shown in Exhibit 3, after two attempts to deliver the documents on October 22, 2006 and on October 23, 2006, the US Postal Service returned the application packet to our office in San Jose, California on January 11, 2007 and it was stamped "UNCLAIMED."

4). As shown in Exhibit 4, on January 15, 2007, I performed a Google Search under Mr. Osman's name and address. I attempted to telephone Mr. Osman at the phone number provided, (781) 440-9065; received recorded message that the number was "no longer in service and there was no additional information." Google displayed Mr. Osman's address as 2906 Village Road West, Norwood, MA 02062.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Respectfully submitted,

Date: 15-JAN-2007

By Peter Zawilski

Peter Zawilski
Registration No. 43,305
(408) 474-9063

Correspondence Address:

NXP, B.V.
Intellectual Property Department
(formerly Philips Intellectual Property & Standards)
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131 USA

CUSTOMER NUMBER: 65913

Exhibit 1

PHILIPS

Richard Keenan
10/17/2006 07:11 AM

To Korne Vennema/SVL/SC/PHILIPS@PHILIPS
cc Jarek Lucek/SVL/SC/PHILIPS@PHILIPS
Peter Zawilski/SVL/IPS/PHILIPS@PHILIPS
bcc
Subject Re: US020555 Patent Application titled, "PRESERVING LINEARITY OF AN ISOLATOR-FREE POWER...and US020557 Patent Application titled, "PRESERVING LINEARITY OF AN ISOLATOR-FREE POWER...
Classification Unclassified

Peter,

I also do not have his contact information.

Rich

Richard Keenan
RFID Applications Engineer - Identification
BU A&I - Sales & Marketing
NXP Semiconductors
2178 Mendon Rd., Suite 300
Cumberland, RI 02864 USA

Tel: +1 401 305 5059
Mob: +1 508 509 1000
Fax: +1 401 305 5060
email: richard.keenan@nxp.com

PHILIPS SEMICONDUCTORS has become NXP SEMICONDUCTORS !!!

Korne Vennema

PHILIPS

Korne Vennema
10/17/06 09:20 AM

To Jarek Lucek/SVL/SC/PHILIPS@PHILIPS
cc Peter Zawilski/SVL/IPS/PHILIPS@PHILIPS
Richard Keenan/SVL/SC/PHILIPS@PHILIPS
Subject Re: US020555 Patent Application titled, "PRESERVING LINEARITY OF AN ISOLATOR-FREE POWER...and US020557 Patent Application titled, "PRESERVING LINEARITY OF AN ISOLATOR-FREE POWER...
Classification Unclassified

Peter,

Unfortunately I do not have his contact information either.

Korné Vennema
Sr. Marketing Application Engineer
NXP Semiconductors

Exhibit 1

2178 Mendon Road, Suite 300
Cumberland, RI 02864
USA

Office Phone: (401) 305-5051, Mobile: (401) 578-0463
Lab Phone: (401) 305-5058 (no voice mail)
Mobile Holland: +31-6-13660653
e-mail: korne.vennema@nxp.com

Jarek Lucek

Jarek Lucek
10/16/06 08:47 PM

To Peter Zawilski/SVL/IPS/PHILIPS@PHILIPS
cc Korne Vennema/SVL/SC/PHILIPS@PHILIPS
Richard Keenan/SVL/SC/PHILIPS@PHILIPS
Subject Re: US020555 Patent Application titled, "PRESERVING LINEARITY OF AN ISOLATOR-FREE POWER...and US020557 Patent Application titled, "PRESERVING LINEARITY OF AN ISOLATOR-FREE POWER...
Classification Unclassified

Hi, Peter,

I don't have contact info for Saleh. Shortly after filing the patents we have let him go.

Korne Vennema or Rich Keenan might have his contact info. I've copied them both on ths email.

Regards,

Jarek Lucek
NXP Semiconductors - founded by Philips
508-446-6739 cell
http://www.semiconductors.com/products/rf/index.html

Peter Zawilski

Peter Zawilski
10/16/06 03:14 PM

To Jarek Lucek/SVL/SC/PHILIPS@PHILIPS
cc
Subject US020555 Patent Application titled, "PRESERVING LINEARITY OF AN ISOLATOR-FREE POWER...and US020557 Patent Application titled, "PRESERVING LINEARITY OF AN ISOLATOR-FREE POWER...
Classification Unclassified

Exhibit 1

Dear Jarek::

I telephoned you earlier in the day and left a message on your voicemail.

I am the Patent Agent managing the above cases, you originally had worked with attorneys in Philips, Briarcliff Manor, New York offices (under Philips IP&S). These cases had been filed in the US Patent Office in December 2003.

I am trying to locate co-inventor Saleh Osman. Apparently, during the filing of the US application he did not sign the Oath & Declaration. Without his signature, the cases will not move forward. You and other co-inventor Richard Keenan had signed.

As of this morning, I have not been able to locate Mr. Osman. Would you happen to have a current E-mail address and telephone number of Mr. Osman?

I appreciate your help.

Hope to hear from you in a day or so.

Kindest regards,

Peter Z

Peter S. Zawilski
Patent Agent

NXP Semiconductors
Intellectual Property Department
Visitor's address: 1130 Ringwood Court; Mail Stop SJ41, San Jose, CA 95131 USA
Courier address: 1140 Ringwood Court; Mail Stop SJ41
San Jose, CA 95131 USA
Mail address: 1109 McKay Drive; Mail Stop SJ41, San Jose, CA 95131 USA
Phone: +1 408 474 9063 Facsimile: +1 408 474-9082
Main Phone: (408) 434-3000
Email: peter.zawilski@philips.com
Intranet: pww.ips.philips.com
Internet: www.nxp.com

Exhibit 2

Peter Zawilski
Patent Agent

Intellectual Property Department
NXP Semiconductors
Tel: +1 408 474 9063, Fax: +1 408 474 9082
1109 McKay Drive, M/S-41, San Jose, CA 95131 USA
peter.zawilski@nxp.com, www.nxp.com

October 19, 2006

Mr. Saleh Osman
2906 Village Road West
Norwood, MA 02062

VIA EXPRESS MAIL

Subject: Philips Filing No.: US 020555; US Application Serial No. 10/538,624, filed 10-JUN-2005
Titled: Preserving Linearity of an Isolator-Free Power Amplifier by Dynamically Switching Active Devices

Dear Saleh:

The above-name patent application was filed in the United Patent Office. Your colleagues Richard Keenan and Jaroslaw Lucek had signed the required papers for completing the filing. However, your signature is necessary for the case to move forward.

I have enclosed a copy of the as filed application for your review. Please sign, date, and return the Oath & Declaration to me at your earliest convenience. A prepaid return envelope has been enclosed. Also, please fax back a copy of both pages to me at (408) 474-9082.

NXP formerly Philips Semiconductors, appreciates your support in protecting its valuable IP assets.

If you have any questions, please feel free to get in touch with me.

Very truly yours,

Peter Zawilski
Patent Agent
(408) 474-9063

Exhibit 2

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)		
☐ Declaration Submitted with Initial Filing OR ☒ Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16(e)) required)	Attorney Docket Number	US 020555
	First Named Inventor	Osman, Saleh
	COMPLETE IF KNOWN	
	Application Number	10/538,624
	Filing Date	06/10/2005
	Group Art Unit	
	Examiner Name	

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Preserving Linearity of an Isolator-Free Power Amplifier by Dynamically Switching Active Devices

(Title of the Invention)

the specification of which:

☐ is attached hereto

OR

☒ was filed on (MM/DD/YYYY) **06/10/2005** as United States Application Number or PCT International Application Number **10/538,624** and was amended on (MM/DD/YYYY) **06/10/2005** (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Numbers(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? Yes	No
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐

☐ Additional foreign application numbers are listed on a supplemental priority data sheet attached hereto:

Exhibit 2

DECLARATION ---- Utilitiy or Design Patent Application

Direct all correspondence to: ☒ Customer Number 24738 AND/OR ☐ Correspondence address below

Name	PHILIPS ELECTRONICS NORTH AMERICA CORPORATION Intellectual Property & Standards		
Address	1109 McKay Drive, M/S-41SJ		
City	San Jose	State California	ZIP 95131
Country	U.S.A	Telephone (408) 474-9073	FAX (408) 474-9082

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

NAME OF SOLE OR FIRST INVENTOR: ☐ A petition has been filed for this unsigned inventor

Given Name (first & middle [if any]) SALEH		Family Name or Surname OSMAN	
Inventor's Signature			Date
Norwood Residence: City	MA State	U.S.A. Country	Great Britain Citizenship
2906 Village Road West Mailing Address			
Norwood City	MA State	02062 ZIP	U.S.A. Country

NAME OF SECOND INVENTOR: ☐ A petition has been filed for this unsigned inventor

Given Name (first & middle [if any]) RICHARD F.		Family Name or Surname KEENAN	
Inventor's Signature			Date
Whitinsville Residence: City	MA State	U.S.A. Country	U.S.A Citizenship
103 Carole Lane Mailing Address			
Whitinsville City	MA State	01588 ZIP	U.S.A. Country

NAME OF THIRD INVENTOR: ☐ A petition has been filed for this unsigned inventor

Given Name (first & middle [if any]) JAROSLAW		Family Name or Surname LUCEK	
Inventor's Signature			Date
Greensboro Residence: City	NC State	U.S.A. Country	U.S.A Citizenship
307 Tower Lane Mailing Address			
Greensboro City	NC State	27410 ZIP	U.S.A. Country

☐ Additional inventors are being named on the _____ supplemental Additional Inventor(s) sheet(s) attached hereto.

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Date In Mo. Day Year	☐ 12 Noon ☐ 3 PM	Postage $	
Time In ☐ AM ☐ PM	Military ☐ 2nd Day ☐ 3rd Day	Return Receipt Fee	
Weight lbs. ozs.	Int'l Alpha Country Code	COD Fee	Insurance Fee
No Delivery ☐ Weekend ☐ Holiday	Acceptance Clerk Initials	Total Postage & Fees $	

DELIVERY (POSTAL USE ONLY)		
Delivery Attempt Mo. Day	Time ☐ AM ☐ PM	Employee Signature
Delivery Attempt Mo. Day	Time ☐ AM ☐ PM	Employee Signature
Delivery Date Mo. Day	Time ☐ AM ☐ PM	Employee Signature

☐ WAIVER OF SIGNATURE (Domestic Only) Additional merchandise insurance is void if waiver of signature is requested. I wish delivery to be made without obtaining signature of addressee or addressee's agent (if delivery employee judges that article can be left in secure location) and I authorize that delivery employee's signature constitutes valid proof of delivery.
NO DELIVERY ☐ Weekend ☐ Holiday
Customer Signature

CUSTOMER USE ONLY
METHOD OF PAYMENT:
Express Mail Corporate Acct. No. X940495
Federal Agency Acct. No. or Postal Service Acct. No.

FROM: (PLEASE PRINT) PHONE ( )
SALEH OSMAN

TO: (PLEASE PRINT) PHONE 474 9067
NXP
1109 MCKAY DRIVE MIS-41SJ
SAN JOSE, CA 95131

PRESS HARD.
You are making 3 copies.
FOR PICKUP OR TRACKING CALL 1-800-222-1811 www.usps.com

867 250 F:02 T:

Exhibit 2

Exhibit 2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

SALEH OSMAN ET AL

Atty. Docket

US020555

Serial No.

Group Art Unit

Filed: CONCURRENTLY

Ex.

PRESERVING LINEARITY OF AN ISOLATOR-FREE POWER AMPLIFIER BY DYNAMICALLY SWITCHING ACTIVE DEVICES

Commissioner for Patents
Alexandria, VA 22313-1450

CERTIFICATE OF EXPRESS MAILING

Express Mail Label No. EV 664 854 860 US

Date of Deposit June 10, 2005

I hereby certify that this paper and/or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. 1.10 on the date indicated above and is addressed to the Commissioner for Patents, PO Box, 1450, Alexandria, VA 22313-1450

Patti DeMichele
Typed Name

Signature

PC JUN 10 2005

Exhibit 2

PTO-1390 (Rev. 02-2005)
App for use through 3/31/2007. OMB 0651-0021
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction [redacted]995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A SUBMISSION UNDER 35 U.S.C. 371		ATTORNEY'S DOCKET NUMBER PHUS020555
		U.S. APPLICATION NO. (If known, see 37 CFR 1.5)
INTERNATIONAL APPLICATION NO. PCT/IB2003/005881	INTERNATIONAL FILING DATE 10 December 2003	PRIORITY DATE CLAIMED 12 December 2002

TITLE OF INVENTION
PRESERVING LINEARITY OF AN ISOLATOR-FREE POWER AMPLIFIER BY DYNAMICALLY SWITCHING ACTIVE

APPLICANT(S) FOR DO/EO/US
SALEH OSMAN, RICHARD F. KEENAN and JAROSLAW LUCEK

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☑ This is a **FIRST** submission of items concerning a submission under 35 U.S.C. 371.
2. ☑ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a submission under 35 U.S.C. 371.
3. ☐ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. ☐ The US has been elected (Article 31).
5. ☑ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☐ is attached hereto (required only if not communicated by the International Bureau).
   b. ☑ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☐ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☑ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☑ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☑ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. ☑ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☑ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☑ A preliminary amendment.
14. ☐ An Application Data Sheet under 37 CFR 1.76.
15. ☐ A substitute specification.
16. ☐ A power of attorney and/or change of address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13*ter*.2 and 37 CFR 1.821- 1.825.
18. ☐ A second copy of the published International Application under 35 U.S.C. 154(d)(4).
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. ☑ Other items or information: Express Mail Certificate; PTO/SB08A; Charge Authorization; Receipt Confirmation Postcard,

Exhibit 2

PTO-1390 (Rev. 02-2005)
Approved for use through 3/31/2007. OMB 0651-0021
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

U.S. APPLICATION NO. (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
	PCT/IB2003/005881	PHUS020555

The following fees have been submitted	CALCULATIONS	PTO USE ONLY
21. ☑ Basic national fee $300	$ 300.00	
22. ☑ Examination fee If International preliminary examination report prepared by USPTO and all claims satisfy provisions of PCT Article 33(1)-(4) ..... $100 All other situations $200	$ 200.00	
23. ☑ Search fee Search fee (37 CFR 1.445(a)(2)) has been paid on the international application to the USPTO as an International Searching Authority ..... $100 International Search Report prepared and provided to the Office ..... $400 All other situations $500	$ 400.00	
TOTAL OF 21, 22 and 23 =	$ 900.00	
☐ Additional fee for specification and drawings filed in paper over 100 sheets (excluding sequence listing or computer program listing filed in an electronic medium). The fee is $250 for each additional 50 sheets of paper or fraction thereof.		
Total Sheets: - 100 = / Extra Sheets: /50 = / Number of each additional 50 or fraction thereof (round up to a whole number) / RATE: x $250	$	
Surcharge of $130.00 for furnishing the oath or declaration later than 30 months from the earliest claimed priority date (37 CFR 1.492(h)).	$	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	18 - 20 =		x $50	$ 0.00	
Independent claims	3 - 3 =		x $200	$ 0.00	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ $360	$	
			TOTAL OF ABOVE CALCULATIONS =	$ 0.00	
☐ Applicant claims small entity status. See 37 CFR 1.27. Fees above are reduced by ½.					
			SUBTOTAL =	$ 900.00	
Processing fee of $130.00 for furnishing the English translation later than 30 months from the earliest claimed priority date (37 CFR 1.492(i)).			+	$	
			TOTAL NATIONAL FEE =	$ 900.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). $40.00 per property			+	$ 40.00	
			TOTAL FEES ENCLOSED =	$ 940.00	
			Amount to be refunded:	$	
			Amount to be charged:	$ 940.00	

a. ☐ A check in the amount of $ _____ to cover the above fees is enclosed.

b. ☑ Please charge my Deposit Account No. 14-1270 in the amount of $ 940.00 to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☑ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 14-1270. A duplicate copy of this sheet is enclosed.

d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the International Application to pending status.

SEND ALL CORRESPONDENCE TO:

Corporate Patent Counsel
Philips Electronics North America Corporation
P.O. Box 3001
Briarcliff Manor, NY 10510

SIGNATURE

Aaron Waxler
NAME

48,027
REGISTRATION NUMBER

Exhibit 2

INFORMATION DISCLOSURE STATEMENT TRANSMITTAL

To Commissioner For Patents
Enclosed herewith is a Form PTO-1449, any required copies of documents listed thereon, and any concise explanation of their relevance is indicated below per 37 CFR 1.97.

Application Number	
Filing Date	CONCURRENTLY
First Named Inventor	SALEH OSMAN ET AL
Group Art Unit	N/A
Examiner Name	N/A
Attorney Docket Number	US020555

☒ Please charge any required fee under §1.17(i) or §1.17(p) or any other required fee (except the issue fee) to Account No. 14-1270.

1. ☐ I certify that these documents were first cited in any communication from a foreign Patent Office in a counterpart foreign application not more than three (3) months ago.

2. ☐ I certify that none of these documents were cited in any communication from a foreign Patent Office in a counterpart foreign application, and, to the knowledge of the undersigned after making reasonable inquiry, none of these documents was known to any individual designated in §1.56(c) more than three (3) months ago.

☐ Applicant hereby petitions under §1.97(d) that this IDS be considered after final Action or Notice of Allowance, pays the fee under §1.17(p) as indicated below, and I certify 1. or 2. as indicated above.

☐ A fee under §1.17(p) is not required under §1.97(c), after the first Action on the merits and more than (3) months after the date of application or RCE, because I certify 1. or 2. as indicated above.

☐ A copy of the citations is not required because they were previously submitted or cited in the parent application (or in U.S. patent application Ser. No._____ Filing Date_____ relied on for an earlier effective filing date under 35 U.S.C. 120).

☒ A copy of the U.S. patent(s) and patent application publication(s) in all U.S. national patent applications filed after June 30, 2003, and in all international applications that have entered the national stage under 35 USC § 371 after June 30, 2003 under 37 CFR 1.491(b), are not required.

☐ A concise explanation of the relevance of each non-English document, as understood by the individual designated in §1.56(c) most knowledgeable about the contents, is enclosed per §1.98(a)(3).

The concise explanation of the relevance of any non-English document, as understood by the individual designated in §1.56(c) most knowledgeable about the contents, is that the document is/was:

☒ cited in the specification or considered in drafting the specification of this application;

☐ previously submitted or cited in the parent application (or in a related patent application Ser. No._____Filing Date:_____);

☐ cited as an "X" or "Y" document in a foreign Patent Office search report in a foreign counterpart application, a copy of which report is also enclosed.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED			
Name (Print Type)	Aaron Waxler	*Registration No. (Attorney/Agent)*	48,027
Signature		*Date*	6/10/05

Exhibit 2

PTO/SB/08A (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	
Filing Date	Concurrently
First Named Inventor	SALEH OSMAN ET AL
Art Unit	N/A
Examiner Name	N/A
Attorney Docket Number	US020555

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 5,423,082	06-06-1995	CYGAN	
		US- 5,442,322	08-15-1995	KORNFELD	
		US- 5,712,593	01-27-1998	BUER	
		US- 6,064,266	05-16-2000	ANDERSON	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Exhibit 2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of | Atty. Docket

SALEH OSMAN ET AL | US020555

Serial No. | Group Art Unit

Filed: CONCURRENTLY | Ex.

PRESERVING LINEARITY OF AN ISOLATOR-FREE POWER AMPLIFIER BY DYNAMICALLY SWITCHING ACTIVE DEVICES

Commissioner for Patents
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Sir:

Prior to calculation of the filing fee and examination, please amend the above-identified application as follows:

Exhibit 2

IN THE SPECIFICATION

Please add the following paragraph before the first paragraph beginning at page 1, line 1:

CROSS REFERENCE TO RELATED APPLICATION

This application claims the benefit of U.S. provisional application serial no. 60/432,896 filed December 12, 2002, which is incorporated herein by reference.

The invention relates to an isolator-free power amplifier circuit typically used in wireless communication devices which preserves linearity of the power amplifier under varying loads. More particularly, linearity is preserved by dynamically adjusting and switching of active devices of the power amplifier circuit.

Exhibit 2

REMARKS

By means of the present amendment, the specification has been amended to include a claim of priority.

In view of the foregoing amendments and remarks, Applicant respectfully requests favorable reconsideration and early passage to issue of the present application.

Respectfully submitted,

By _____
Aaron Waxler, Reg. 48,027
Attorney
(914) 333-9608

Exhibit 2

PTO/SB/01 (03-01)
Approved for use through 10/31/2002. OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

☒ Declaration Submitted With Initial Filing OR ☐ Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16 (e)) required)

Attorney Docket Number	PH[redacted]020555
First Named Inventor	SALEH OSMAN
COMPLETE IF KNOWN	
Application Number	/
Filing Date	
Group Art Unit	
Examiner Name	

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

PRESERVING LINEARITY OF AN ISOLATOR-FREE POWER AMPLIFIER BY DYNAMICALLY SWITCHING ACTIVE DEVICES

the specification of which *(Title of the Invention)*

☒ is attached hereto

OR

☐ was filed on (MM/DD/YYYY) [ ] as United States Application Number or PCT International Application Number [ ] and was amended on (MM/DD/YYYY) [ ] (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY) Country	Priority Not Claimed	Certified Copy Attached? YES	NO
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐

☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto:

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DECLARATION — Utility or Design Patent Application

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Philips Electronics North America Corporation **Name**			
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BRIARCLIFF MANOR **City**	NY **State**	10510 **ZIP**	
U.S.A. **Country**	(914) 945-6000 **Telephone**	(914) 332-0615 **Fax**	

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

NAME OF SOLE OR FIRST INVENTOR: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any]) SALEH		**Family Name or Surname** OSMAN	
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2906 VILLAGE ROAD WEST **Mailing Address**			
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Inventor's Signature R. F. Keenan		**Date** 3/5/04	
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~~280 VILLAGE STREET UNIT G1~~ 103 Carole lane R.K. **Mailing Address**			
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☐ **Additional Inventors are being named on the 1ST PAGE** supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto.

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DECLARATION

ADDITIONAL INVENTOR(S)
Supplemental Sheet
Page 1 of 1

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor		
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Mailing Address 40 GREEN MEADOW LANE			
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City CUMBERLAND	**State** RI	**ZIP** 02864	**Country** USA

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor		
Given Name (first and middle [if any])	Family Name or Surname		
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COMPLETE IF KNOWN	
Application Number	/
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Group Art Unit	
Examiner Name	

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

PRESERVING LINEARITY OF AN ISOLATOR-FREE POWER AMPLIFIER BY DYNAMICALLY SWITCHING ACTIVE DEVICES

(Title of the Invention)

the specification of which

☒ is attached hereto

OR

☐ was filed on (MM/DD/YYYY) ____ as United States Application Number or PCT International Application Number ____ and was amended on (MM/DD/YYYY) ____ (if applicable).

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U.S.A. **Country**	(914) 945-6000 **Telephone**	(914) 332-0615 **Fax**	

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Given Name (first and middle [if any]) RICHARD F.		**Family Name or Surname** KEENAN	
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PRESERVING LINEARITY OF AN ISOLATOR-FREE POWER AMPLIFIER BY DYNAMICALLY SWITCHING ACTIVE DEVICES

The invention relates to an isolator-free power amplifier circuit typically used in wireless communication devices which preserves linearity of the power amplifier under varying loads. More particularly, linearity is preserved by dynamically adjusting and switching of active devices of the power amplifier circuit.

Power amplifiers are used in transmitters to amplify signals, such as radio frequency (RF) signals. Such power amplifiers are included in transmitters of wireless communication devices, such as mobile telephones. The power amplifier typically provides an amplified RF signal to an antenna for transmission over the air.

RF antennas as for instance applied in mobile phones, operate in strongly varying environments, resulting in a varying antenna input impedance, a VSWR (Voltage Standing Wave Ratio) of 4:1 is not uncommon. Especially at high output levels, this may result in a severe distortion of for instance a CDMA (code division multiple access), TDMA (time division multiple access), Edge or W-CDMA modulated carrier signal having a non-constant envelope.

The conventional solution to protect the power amplifier of a cellular phone against antenna mismatch conditions to preserve linearity is to use an isolator, such as a circulator, placed between the power amplifier and the output load, such as the antenna, to limit the effects of load impedance variation on the performance of the power amplifier. The circulator secures proper 50 Ohm loading of the power amplifier under antenna mismatch conditions by dissipating the reflected power in the isolator or in a third circulator port termination. Directivity in the power flow is created by ferromagnetic material.

The above aspects of the state of the art are described in more detail with reference to Fig. 1 which shows a basic block diagram of an arrangement 10 used for a power source 12 isolated with a circulator 14 from a mismatched antenna 16. A current source 18 and its impedance Z_o represent an ideal power source (RF-transistor) 12. A matching circuit 20 is connected between the antenna 16 and power source 12, with another terminal 22 connected to ground.

Exhibit 2

Part of the power P_{inc_circ} from the matching circuit 20 to the circulator 14 is delivered as P_{inc_ant} to the antenna 16 where some power is reflected back P_{refl_ant} to the circulator 14. Thanks to the circulator 14, the reflected power P_{refl_ant} from the antenna 16 is not reflected towards the source 12, but dissipated into the circulator load P_{diss}. Consequently, the reflected power P_{refl_circ} from the circulator 14 and the reflected power P_{refl_source} from the matching circuit 20 towards the source 12 are zero. This avoids extremes that would occur when incident and reflected waves add up in-phase. However, since it is desired to preserve power amplifier linearity and maintain Prad constant (under control of field strength indication at the base station), then the incident power P_{inc_source} from the source 12 has to be increased, thus increasing power dissipation, to overcome reflection losses resulting in enhanced signal voltage and current at the source 12. Thus, the circulator 14 only partly preserves power amplifier linearity under antenna mismatch conditions. In addition, power dissipation and consumption remains high thus requiring battery charging and decreasing battery life of the mobile phone as well as decreasing efficiency.

It is desirable to remove the isolator or circulator 14 connected to the antenna 16. However, removal of the isolator allows load impedance variations to detrimentally affect the performance, e.g., linearity, of the power amplifier. Accordingly, there is a need to have a power amplifier circuit where the isolator is removed yet the performance and linearity of the amplifier is preserved despite load impedance variations.

According to the invention, linear power output of a power amplifier is substantially maintained despite load variations and having no isolator connected to the load. This is achieved by switching, such as selectively and independently switching, in or out active devices as a function of the difference between the forward and reflected power.

In one embodiment according to the present invention, an amplifier circuit for preserving linearity of an amplifier is provided. The amplifier circuit may be used in wireless communication devices, for example. The amplifier circuit includes a driver stage having a first set of active devices which receive a signal for pre-amplification and output a pre-amplified signal. An output stage has a second set of active devices which receive the pre-amplified signal for further amplification and output an amplified signal. A detector measures levels of forward signal and reflected signal of the amplified signal. The amplifier circuit also includes a control circuit which controls turning on and off or

Exhibit 2

switching the first and/or second set of active devices as a function of the levels of forward and reflected signals to substantially maintain linearity of the amplifier circuit with load variations. For example, the control circuit selectively and independently turns on and off each of the active devices included in the first and second set of active devices.

In another embodiment according to the present invention, a method for substantially preserving linearity of an amplifier under varying loads is provided. The method includes measuring levels of forward and reflected signals at the amplifier output; and selectively and independently turning on and off a first set of active devices of a driver stage and/or a second set of active devices of an output stage of the amplifier circuit as a function of the measured levels, such as the difference or ratio of the measured forward and reflected signals, to substantially maintain linearity of the amplifier circuit with load variations. For example, the turning on/off act selectively and independently turns on and off each of the active devices of the first and /or second set of active devices.

Further features and advantages of the invention will become more readily apparent from a consideration of the following description.

The accompanying drawings specify and show preferred embodiments of the invention, wherein like elements are designated by identical references throughout the drawings; and in which:

Fig. 1 shows a prior art block diagram of a power source isolated with a circulator from a mismatched antenna;

Fig. 2 shows a wireless communication system according to the present invention;

Fig. 3 shows an isolator-free amplifier circuit according to the present invention;

Fig. 4 shows a flow chart of a method for preserving performance, e.g., linearity, of an isolator-free amplifier circuit according to the present invention; and

Fig. 5 shows a summarized flow chart of the method for preserving performance, e.g., linearity, of an isolator-free amplifier circuit according to the present invention.

The invention, together with attendant advantages, will be best understood by reference to the following detailed description of the preferred embodiment of the invention, taken in conjunction with the accompanying drawing.

An amplifier circuit for use in wireless communication devices for example is described where, illustratively, an RF power amplifier is used in RF antenna circuits. In the following description, numerous specific details are set forth, such as specific type and

Exhibit 2

number of transistors, in order to provide a thorough understanding of the present invention. However, it will be obvious to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well known circuits have not been set forth in detail in order to not unnecessarily obscure the present invention.

The wireless communication device may be for example a mobile cellular or cordless telephone, pager, an Internet appliance or other consumer devices, and is typically part of a communication system. Fig. 2 shows a wireless communication system, such as a mobile telephone system 40 comprising a primary or base station (BS) 50 and a plurality of secondary or mobile stations (MS) 60. The BS 50 comprises a network controller 52, such as a computer, coupled to a transceiver 54 which is in turn coupled to radio transmission means such as an antenna 56. A connection means such as a wire 58 couples the controller 52 to a public or a private network.

Each MS 60 comprises a processor 62 such as a micro-controller (μC) and/or a digital signal processor (DSP). Typically, the DSP processes voice signals, while the μC manages operation of the MS 60. The processor 62 is coupled to a transceiver means 64 coupled to radio transmission means, e.g., an antenna 66. A memory 68, such as an EPROM and RAM, is coupled to the processor 62 and stores data related to operation and configuration of the MS 60. Communication from the BS 50 to MS 60 takes place on a downlink channel 72, while communication from the MS 60 to BS 50 takes place on an uplink channel 74. The MS 60 also includes a user interface such as a keyboard and a screen, as well as a microphone coupled to the transmit branch or section of the transceiver 64 and a speaker coupled to the receiver section of the transceiver 64.

The transmit section of the transceiver 64 transmits signals over the uplink channel 74, which the receive branch of the transceiver 64 receives signals over the downlink channel 72. The transceiver 64 includes a selection means to selectively couple a power amplifier (PA) of the transmit section or a low noise amplifier (LNA) of the receive section to the antenna 66. Illustratively, the selection means includes a duplexer or bandpass filters tuned to the transmit and receive frequency ranges, respectively. As is well known in the art, the transceiver 64 also includes other circuits such as a down converter for converting the received radio frequency (RF) signals to intermediate frequency and/or baseband signals, and demodulator/decoder in the receive branch. By contrast, the transmit branch

Exhibit 2

of the transceiver 64 includes an up converter and a modulator/encoder. Converters that convert between analog and digital formats are also typically present in the transceiver 64.

Fig. 3 shows an embodiment of an amplifier circuit 100 according to the present invention which is illustratively used as a power amplifier circuit to amplify RF signals in wireless communication devices. For example, the amplifier circuit 100 is part of the transceiver 64 of the MS 60 shown in Fig. 2, and more particularly, in the transmit branch of the transceiver 64. Typically, the input of the amplifier circuit is coupled to a modulator and receives modulated RF signals for amplification. The amplifier output is coupled to a load, such as the antenna 66, where the amplified RF signals are transmitted over the air on the uplink channel 74 for example.

As shown in Fig. 3, the amplifier circuit 100 comprises an input match circuit 110 for buffering the input of the amplifier circuit 100 and matching its input impedance with the output impedance of the circuit coupled thereto, such as a modulator. The output of the input match circuit 110 is coupled to a driver stage 120 through DC blocking capacitors 130. The signal to be amplified, such as a modulated signal, is provided by the input match circuit 110 to the capacitors 130, which substantially block DC components and provide a signal substantially without a DC offset to the driver stage 120.

The driver stage 120 comprises a plurality of active devices, such as transistors 140, which receive the substantially DC-free signal from the capacitors 130 for pre-amplification to a first level. Illustratively, three pre-amplification bipolar transistors, such as NPN transistors 140 are used, each having a base coupled to a respective capacitor 130. Each base is further independently coupled to a bias control circuit 145 for providing a proper DC biasing signal. This allows the bias control circuit 145 to independently and selectively control, e.g., turn on or off, each transistor 140. The emitter of each transistor 140 is coupled to ground, while the output or collector of each transistor 140 is coupled to an inter-stage match circuit 150 for buffering and impedance matching between the output of driver stage 120 and input of an output stage 160.

The pre-amplified signal from the driver stage 120 is provided to the input of the output stage 160 through the inter-stage match circuit 150, and DC blocking capacitors 170 for substantially blocking DC signals similar to the DC blocking capacitors 130.

The output stage 160 is similar to the driver stage 120 and also comprises a plurality of transistors 180 which receive the substantially DC-free signal from the

Exhibit 2

capacitors 170 for amplification to the output level. Illustratively, three amplification NPN transistors 180 are used, each having a base coupled to a respective capacitor 170. Each base is further independently coupled to the bias control circuit 145 for providing the proper DC biasing signal. This allows the bias control circuit 145 to independently and selectively control, e.g., turn on or off, each transistor 180. Thus, all the control ports of the active devices, e.g., all the bases of the transistors 140, 180 are independently coupled to the bias control circuit 145 allowing it to independently and selectively control each of the transistors 140, 180, thus adjusting the amplification or gain of the driver and output stages 120, 160. The emitter of each transistor 180 is connected to ground, while the output or collector of each transistor 180 is directly or indirectly coupled to the load without any isolation therebetween. Further, the emitter area of each active device 140, 180 is selected such that optimum performance is achieved for a given load, inter-stage and source condition.

By way of example, suppose a power amplifier is to deliver 30 dBm of output power to a 50 ohm load. If the power amplifier's final stage's output has peak voltage swing of 1.4 volts for linear operation, then a loss-less impedance matching network separating load and power amplifier must have an impedance transformation ratio of 51:1.

Consider a worst case mismatch condition over all phases of a constant VSWR. The two impedance extremes are high and low loads. In the former case, large voltage swings develop across the output of the final stage causing non-linearity in the form of clipping due to the onset of high AC impedance. In the later case, the demand for output current elevates due to the onset of low AC impedance. By monitoring the incident and reverse power levels, a measurement of the impedance condition is obtained as shown in block 200 of Fig. 4. In block 210, the impedance level or mismatch is checked and if a normal or matched level is obtained, then normal matched operation is continued in block 220. If the impedance level or mismatch is not normal as determined in block 210, then it is determined in block 230 whether the difference or ratio of the measured forward and reflected signals is high or low. If it is high, indicating a relatively high forward signal, then in block 240 less active area is switched by switching in less transistors, for example. If the determined in block 230 indicates that the difference or ratio of the measured forward and reflected signals is low, indicating a relatively low forward signal, then in block 250 more active area is switched by switching in more transistors, for example.

Exhibit 2

Illustratively, the active area is switched from more to less for a low to high load impedance variation in accordance with the desired output power and linearity. Next, the impedance condition is re-measured by returning to block 200 and the operations are repeated until a matched level is obtained in block 210 and normal matched operation is continued in block 220. The monitoring and measurement of the impedance in block 200 are continuously or intermittently checked and adjustments are made, if needed, to arrive to the matched condition of block 220.

Returning to Fig. 3, a detector, such as a power detector 190, is also coupled to the output of each transistor 180 for detecting the level, e.g., the power level, of the amplified RF signal at the output of the output stage 160. The power detector 190 is in turn coupled to the bias control circuit 145. The output of the amplifier circuit 100 is coupled to an antenna without an isolator therebetween.

The power detector 190 provides the DC bias control circuit 145 a measure of the forward and reflected output power of the amplifier circuit 100. As a function of the forward and reflected power levels, the DC bias control circuit 145 independently and selectively controls each of the respective transistors 140, 180 of the driver and output stages 120, 160 to substantially maintain the optimum performance and constant linearity of the amplifier circuit 100 despite variations in the impedance of the load connected to the output of the amplifier circuit 100. In particular, the bias control circuit 145 turns on or off each active device independently by providing the proper direct current (DC) biasing at the base of each of the active devices 140, 180, thus switching in more or less active devices 140, 180 in response to the difference between the forward and reflected power level.

As is well known by one skilled in the art, the changes in the forward and reflected power levels measured by the power detector 190 are related to changes in the load impedance, e.g., the impedance of the antenna 66 shown in Fig. 2. In particular, for a load impedance substantially matched to the output impedance of the output of the amplifier circuit 100, the ratio or the difference between the forward and reflected power levels is high, while it is low for substantially mismatched impedances. U.S. Patent No. 5,423,082, which is incorporated herein by reference in its entirety, discloses a transmitter that includes a closed loop feedback to compensate for varying antenna loads without an isolator, which is accomplished by taking the reflected output energy into account to maintain a constant overall loop gain by adjusting the gain of variable gain stages.

Exhibit 2

Bias control circuits are also well known in the art, such as the bias control circuit disclosed in U.S. Patent Nos. 5,442,322 and 5,712,593 which are incorporated herein by reference in its entirety. In U.S. Patent No. 5,442,322, a bias control circuit compares a bias control voltage with a value indicative of the current in an active device and provides a control signal to the control terminal of the active device to control the operating point thereof. The bias point of a power amplifier is similarly controlled in U.S. Patent No. 5,712,593 by a control circuit in response to comparing a reference value to a filtered portion of the RF output signal. Changing the amplifier bias point limits the effect of the load impedance variation on the amplifier performance. U.S. Patent No. 6,064,266, which is incorporated herein by reference in its entirety, is also related to limiting the effect of the load impedance variation on the amplifier performance, which is achieved by modifying the RF output signal path, instead of the DC bias, by switching in a resistor in parallel with the output impedance when a threshold detector detects variations in the load impedance above a predetermined value.

The bias control circuit 145 of the present amplifier circuit 100 may include a processor or a comparator for comparing the values of forward and reflected power levels measured by the power detector 190 with at least one threshold value. Based on the comparison, the DC bias control circuit 145 selectively and independently controls turning on or off the transistors 140, 180 of the driver and output stages as necessary, namely, as a function of the levels of the forward and reflected signals, to substantially maintain constant the linearity of the amplifier circuit 100 with load variations.

Fig. 5 shows a flow chart 300 of a method for preserving performance of an isolator-free amplifier circuit according to the present invention. In block 310, the power detector measures the forward and reflected power levels at the output of the amplifier circuit and provides this information to the bias control circuit 145. In response to the measured forward and reflected power levels, such as their difference or ratio values, in block 320, the control circuit 145 selectively and independently turns on or off the active devices 140, 160, such as by providing proper DC biasing, to substantially maintain optimal performance and constant linearity of the amplifier circuit 100 shown in Fig. 3.

While the present invention has been described in particular detail with reference to specific exemplary embodiments thereof, it should also be appreciated that numerous modifications and changes may be made thereto without departing from the broader and

Exhibit 2

intended spirit and scope of the invention as set forth in the claims that follow. The specification and drawings are accordingly to be regarded in an illustrative manner and are not intended to limit the scope of the claims which follow.

Exhibit 2

CLAIMS:

1. An amplifier circuit comprising:

a driver stage having first active devices which receive a signal for pre-amplification and output a pre-amplified signal;

an output stage having second active devices which receive said pre-amplified signal for further amplification and output an amplified signal;

a detector which measures levels of forward signal and reflected signal of said amplified signal; and

a control circuit which controls turning on and off of said first active devices and said second active devices as a function of said levels of forward signal and reflected signal to substantially maintain linearity of said amplifier circuit with load variations.

2. The amplifier circuit of claim 1, wherein said output stage is coupled to a load without an isolation device between said output stage and said load.

3. The amplifier circuit of claim 1, wherein said control circuit independently controls each of said first active devices and said second active devices.

4. The amplifier circuit of claim 1, wherein said control circuit independently controls each of said first active devices.

5. The amplifier circuit of claim 1, wherein said control circuit independently controls each of said second active devices.

6. The amplifier circuit of claim 1, wherein said first active devices and said second active devices are NPN transistors.

7. The amplifier circuit of claim 1, further comprising an input match circuit coupled between an input of said amplifier circuit and said driver stage for matching an input impedance of said amplifier circuit to an output impedance of a device coupled to said input.

Exhibit 2

8. The amplifier circuit of claim 7, further comprising at least one capacitor coupled between said input match circuit and said driver stage.

9. The amplifier circuit of claim 1, further comprising at least one capacitor coupled between an input of said amplifier circuit and said driver stage.

10. The amplifier circuit of claim 1, further comprising an inter-stage match circuit coupled between an output of said driver stage and an input of said output stage for matching an input impedance of said output stage to an output impedance of said driver stage.

11. The amplifier circuit of claim 10, further comprising at least one capacitor coupled between said inter-stage match circuit and said output stage.

12. The amplifier circuit of claim 1, further comprising at least one capacitor coupled between said inter-stage match circuit and said output stage.

13. A wireless communication device comprising the amplifier circuit of claim 1.

14. An amplifier circuit comprising:

a driver stage having a first set of active devices which receive a signal for pre-amplification and output a pre-amplified signal;

an output stage having a second set of active devices which receive said pre-amplified signal for further amplification and output an amplified signal;

a detector which measures levels of forward signal and reflected signal of said amplified signal; and

a control circuit which independently and selectively controls switching each active device of said first set of active devices and said second set of active devices as a function of said levels of forward signal and reflected signal to substantially maintain linearity of said amplifier circuit with load variations.

Exhibit 2

15. A method for substantially maintaining linearity of an amplifier circuit with variations of a load coupled to an output of said amplifier circuit comprising:

measuring levels of forward signal and reflected signal at said output; and

turning on and off first active devices of a driver stage of said amplifier circuit and second active devices of an output stage of said amplifier circuit as a function of said levels.

16. The method of claim 15, wherein said turning act independently turns on and off each of said first active devices and said second active devices.

17. The method of claim 15, wherein said turning act independently turns on and off each of said first active devices.

18. The method of claim 15, wherein said turning act independently turns on and off each of said second active devices.

Exhibit 2

ABSTRACT

An amplifier circuit (100) includes a driver stage (120) with active devices (140) for pre-amplification and output of a pre-amplified signal; and an output stage (160) with active devices (180) for further amplification of the pre-amplified signal and output of an amplified signal. A detector (190) measures levels of forward and reflected parts of the amplified signal, and a control circuit (145) independently and selectively controls turning on and off of the active devices (140, 180) of the driver and output stages (120, 160) as a function of the levels of the forward and reflected signals to substantially maintain linearity of the amplifier circuit (100) with load variations.

Exhibit 2

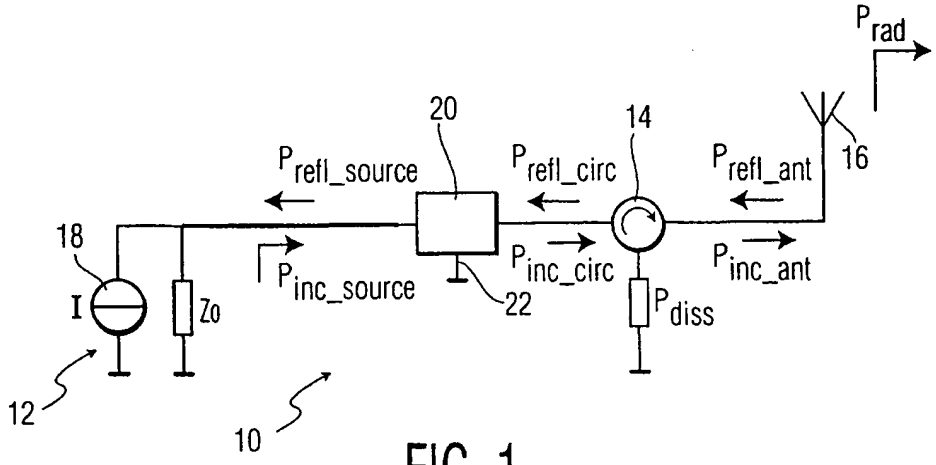

FIG. 1

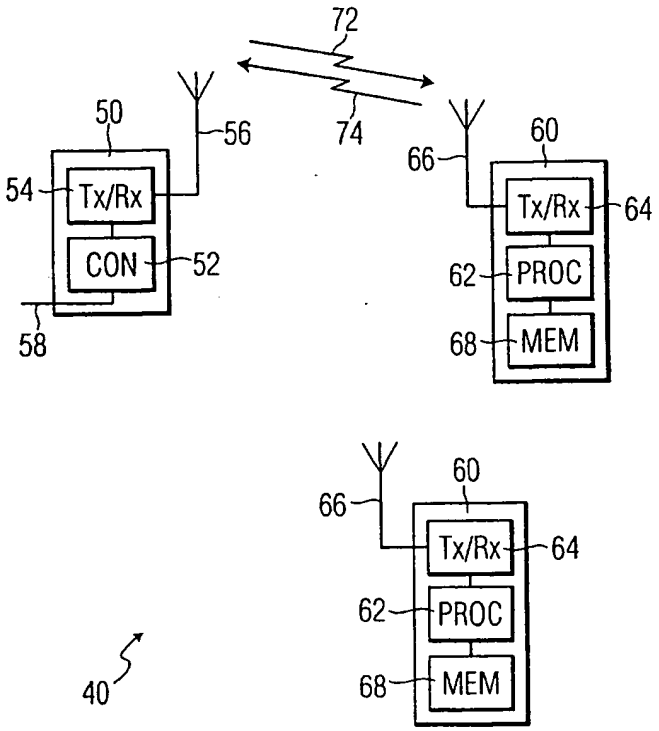

FIG. 2

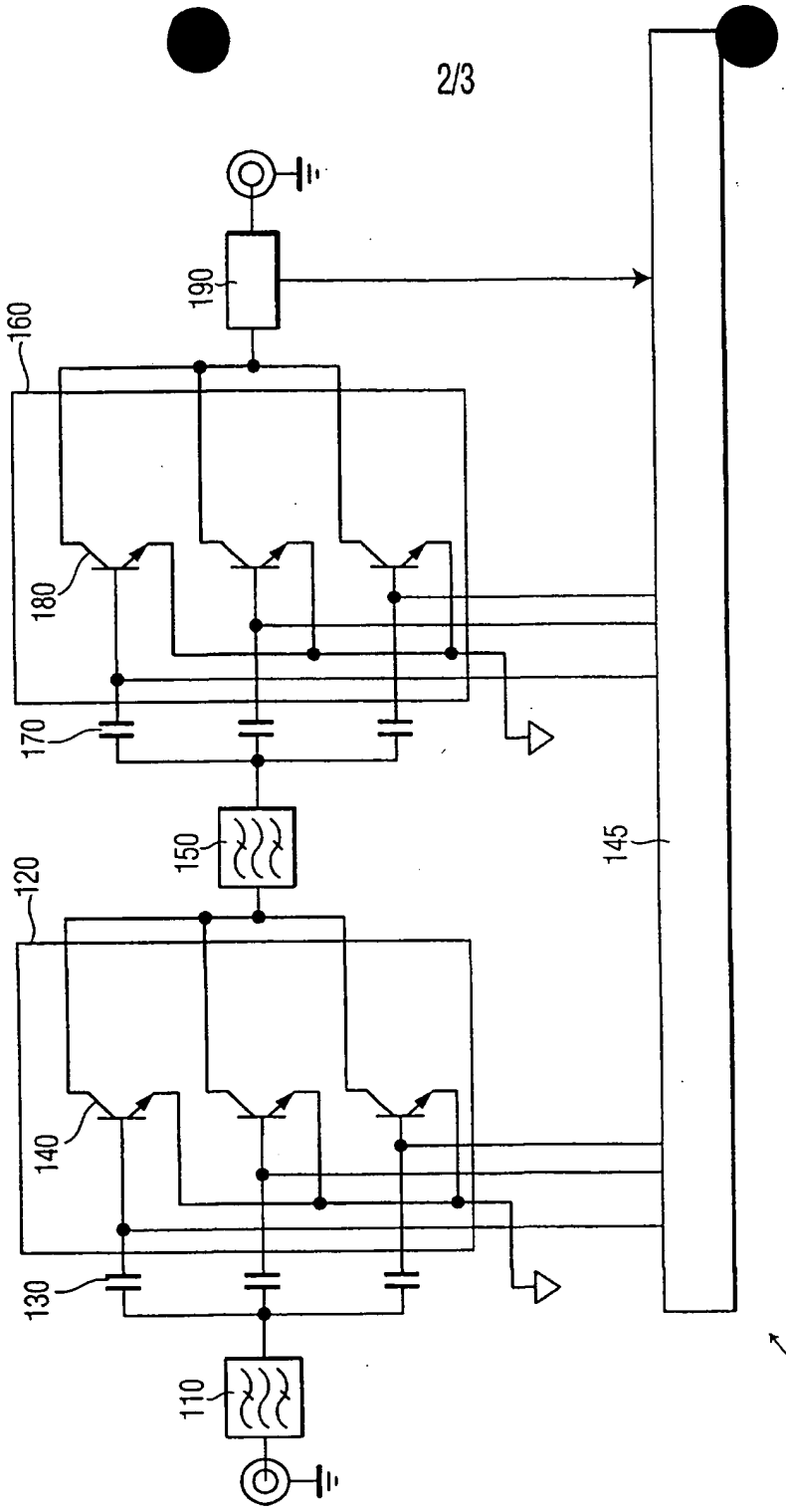

FIG. 3

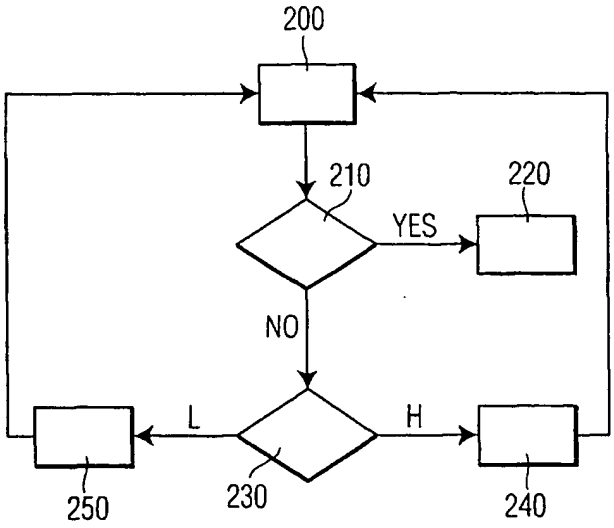

FIG. 4

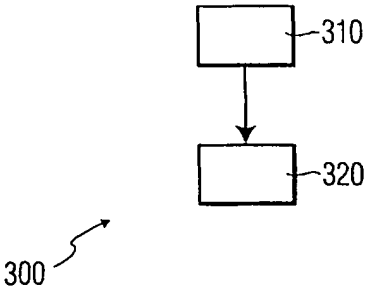

FIG. 5

Exhibit 2

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In re Application of

SALEH OSMAN ET AL

Serial No.

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US020555

Group Art Unit

Ex.

PRESERVING LINEARITY OF AN ISOLATOR-FREE POWER AMPLIFIER BY DYNAMICALLY SWITCHING ACTIVE DEVICES

Commissioner for Patents
Alexandria, VA 22313-1450

AUTHORIZATION PURSUANT TO 37 CFR 1.136(a)(3)
AND TO CHARGE DEPOSIT ACCOUNT

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The Commissioner is hereby requested and authorized to treat any concurrent or future reply in this application requiring a petition for extension of time for its timely submission, as incorporating a petition for extension of time for the appropriate length of time.

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Respectfully submitted,

By_____
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